



SREE VAHINI INSTITUTE OF SCIENCE AND TECHNOLOGY

ONE DAY GUEST LECTURE ON

“DESIGN PRINCIPLES OF LOW POWER VLSI”

30th JANUARY-2025

Venue: Main Seminar Hall, SVIST

Organized By

Department of Electronics & Communications Engineering

Resource Person from

Dr.K.Mariya Priyadarshini


CO-ORDINATOR


HOD


PRINCIPAL



SREE VAHINI INSTITUTE OF SCIENCE & TECHNOLOGY

Approved by AICTE and affiliated to JNTUK

Behind Ganesh Temple, Sai Vahini Nagar, By Pass Road, TIRUVURU- 521235, Krishna Dt., A.P.

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visit us: www.sreevahini.edu.in

Date: 30-01-2025

To,

Dr. K. Mariya Priyadarshini

Professor

ALIET, VIJAYAWADA

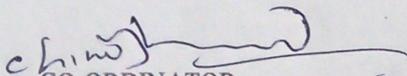
Subject: Letter of Appreciation

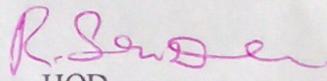
Dear Madam,

Thank you for your support in conducting the One Day guest lecture on “**DESIGN PRINCIPLES OF LOW POWER VLSI**” an interactive session for sharing entrepreneurial Knowledge as a resource person and spending your valuable time with us. The workshop attendees had the unique opportunity to learn from the knowledge imparted and suggestions expressed by you.

We look forward to your continued support and association with Dept. of ECE, SVIST in all our future endeavors.

With warm regards,


CO-ORDINATOR


HOD


Principal



SREEVAHINIINSTITUTE OFSCIENCE&TECHNOLOGY

Bypass Road, Sri Vahini Nagar, Tiruvuru-521235, Krishna Dt. A.P

SVIST/ECE/Circular/2025

24-01-2025

CIRCULAR

It is planned to conduct One day Guest lecture Programming “**DESIGN PRINCIPLES OF LOW POWER VLSI**” II, III & IV B. TECH Students on 30-01-2025. Hence students are informed to attend the program without fail

Venue: Main Seminar Hall

Time: 9:30 am to 4:30 pm


Co-Ordinator


HOD


Principal

Copy to:

1. Faculty circulation
2. All classrooms (II, III, IV B. TECH)
3. Notice Board
4. File



SREE VAHINI INSTITUTE OF SCIENCE AND TECHNOLOGY
AUTONOMOUS

Tiruvuru (V), Tiruvuru (M), NTR (DT), AP 521235.

Name of the Guest Lecture on : DESIGN PRINCIPLES OF LOW POWER VLSI

Department : Electronics and Communication Engineering

Date : 30-01-2025

Venue : Main Seminar Hall, SVIST

Number of participants : 250

Resource Person : Dr.K.Mariya Priyadarshini

Objective

Low Power VLSI design principles aim to reduce dynamic (switching) and static (leakage) power in integrated circuits for better battery life, less heat, and lower costs, with objectives including minimizing voltage (V_{dd}) via scaling, reducing switching activity using clock gating/power gating, optimizing capacitance, and controlling leakage with multi-V_t design, all crucial for portable and high-performance systems.

Workshop overview

A Guest Lecture on “**DESIGN PRINCIPLES OF LOW POWER VLSI**” on was organized by the Department of Electronics & Communication Engineering Technology through offline mode for II, III B.TECH & IV B.TECH students. The inauguration of the Guest Lecture started at 10:00 AM in Seminar Hall the dignitaries were **Dr.K.Mariya Priyadarshini**, Professor, Dept of ECE, **Andhra Loyola Institute of Engineering and Technology Vijayawada**.

A Guest Lecture on **DESIGN PRINCIPLES OF LOW POWER VLSI**” Clock distribution, different types of voltage scaling, Gate level optimization technique, multi VDD technique, Power Gating and various low power techniques used in the industry were discussed. He concluded the talk with a brief explanation on the design elements required to design low-power SoCs with Retention Flip Flop and level shifters.



Chinn
CO-ORDINATOR

R. Srinivas
HOD

[Signature]
PRINCIPAL